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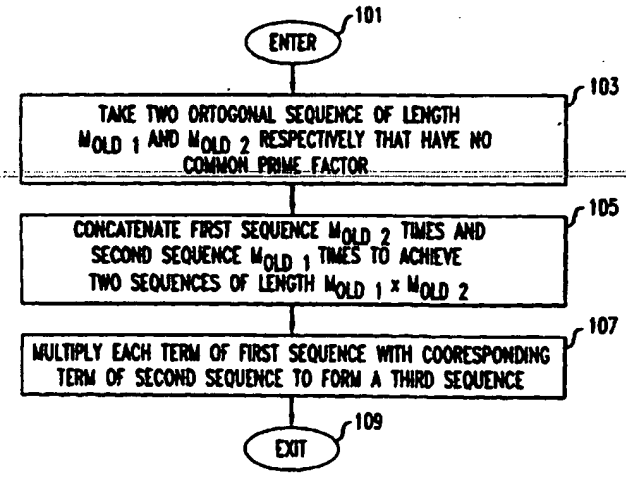
(54) Training sequences for low-latency LMS implementation

(57) Use of a training sequence having terms that are orthogonal to each other are employed to considerably speed up execution of the LMS algorithm. Such orthogonal sequences are developed for a channel that is described as a finite impulse response (FIR) filter having a length M_{new} from the already existing orthogonal training sequences for at least two channels that have respective lengths M_{old1} and M_{old2} each that is less than M_{new} such that the product of M_{old1} and M_{old2} is equal to M_{new} when M_{old1} and M_{old2} have no common prime number factor. More specifically, a set of initial existing orthogonal training sequences is found, e.g., using those that were known in the prior art or by performing a computer search over known symbol constellations given a channel of length M. Thereafter, an orthogonal training sequence of length M_{new} is developed, where the product of M_{old1} and M_{old2} is equal to M_{new} by repeating the training sequence old1 M_{old2} number of times to form a first concatenated sequence and repeating the training sequence old2 M_{old1} number of times to form a second concatenated sequence, so that both the first concatenated sequence and the second concatenated sequence have the same length. Each term of the first concatenated sequence is multiplied by the correspondingly located term in the second concatenated sequence which is placed in the same location in a new sequence made up of the resulting M_{new} products. This new sequence is an orthogonal sequence of length M_{new}.

FIG. 1



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Description

Technical Field

[0001] This invention relates to the art of training a receiver that receives signals from a channel that introduces noise and intersymbol interference, and in particular, to a system of generating the training sequence so that training may be performed using the least mean squares (LMS) algorithm with low latency.

Background of the Invention

[0002] A problem in the art of training a receiver that a) receives signals from a channel that introduces noise and intersymbol interference and b) which uses the least mean squares (LMS) algorithm, is that the high speed of computation required to perform the LMS algorithm limits the transmission rate for data. Therefore, the prior art uses a small step size so that the computation is approximately the same as if the elements of the training sequence were orthogonal. However, this approach leads to a coarser channel estimate, and the training takes longer than is desirable due to the small step size.

Summary of the Invention

[0003] I have recognized that if the terms of the training sequence could actually be orthogonal to each other then the LMS algorithm can be speeded up considerably. Some orthogonal sequences have been found, but these are limited to particular conditions, e.g., certain lengths or the modulation scheme for which they could be used do not correspond to conventionally used modulation arrangements. However, there has been no method to develop training sequences that indeed have orthogonal terms given the number of weights needed to properly describe the channel as a finite impulse response (FIR) filter.

[0004] Therefore, in accordance with the principles of the invention, I have devised a process by which an orthogonal training sequence can be developed for a channel that is described as a finite impulse response (FIR) filter having a length M_{new} from the already existing orthogonal training sequences for at least two channels that have respective lengths M_{old1} and M_{old2} each that is less than M_{new} such that the product of M_{old1} and M_{old2} is equal to M_{new} when M_{old1} and M_{old2} have no common prime number factor. More specifically, a set of initial existing orthogonal training sequences is found, e.g., using those that were known in the prior art or by performing a computer search over known symbol constellations given a channel of length M. Thereafter, an orthogonal training sequence of length M_{new} is developed, where the product of M_{old1} and M_{old2} is equal to M_{new} by repeating the training sequence old1 M_{old2} number of times to form a first concatenated sequence and repeating the training sequence old2 M_{old1} number of times to form a second concatenated sequence, so that both the first concatenated sequence and the second concatenated sequence have the same length. Each term of the first concatenated sequence is multiplied by the correspondingly located term in the second concatenated sequence which is placed in the same location in a new sequence made up of the resulting M_{new} products. This new sequence is an orthogonal sequence of length M_{new}. If there is more than one existing orthogonal sequence for a particular length channel, e.g., there may be different orthogonal sequences for different modulation schemes for the same length channel, the implementer may choose which ever orthogonal sequence gives the results desired. Often, for practical applications, the result that yields the modulation scheme that is most suitable for use with the actual channel, which may yield the highest speeds, or the result that yields the smallest alphabet, which would reduce the hardware required for implementation, is desirable.

[0005] Advantageously, a receiver using such an orthogonal training sequence may employ the optimum step size, resulting in the fastest training.

Brief Description of the Drawing

[0006] In the drawing:

FIG. 1 shows, in flowchart form, an exemplary process for developing an orthogonal training sequence in accordance with the principles of the invention; and

FIG. 2 shows an exemplary receiver arranged in accordance with the principles of the invention.

Detailed Description

[0007] The following merely illustrates the principles of the invention. It will thus be appreciated that those skilled in the art will be able to devise various arrangements which, although not explicitly described or shown herein, embody

the principles of the invention and are included within its spirit and scope. Furthermore, all examples and conditional language recited herein are principally intended expressly to be only for pedagogical purposes to aid the reader in understanding the principles of the invention and the concepts contributed by the inventor(s) to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions. Moreover, all statements herein reciting principles, aspects, and embodiments of the invention, as well as specific examples thereof, are intended to encompass both structural and functional equivalents thereof. Additionally, it is intended that such equivalents include both currently known equivalents as well as equivalents developed in the future, i.e., any elements developed that perform the same function, regardless of structure.

[0008] Thus, for example, it will be appreciated by those skilled in the art that any block diagrams herein represent conceptual views of illustrative circuitry embodying the principles of the invention. Similarly, it will be appreciated that any flow charts, flow diagrams, state transition diagrams, pseudocode, and the like represent various processes which may be substantially represented in computer readable medium and so executed by a computer or processor, whether or not such computer or processor is explicitly shown.

[0009] The functions of the various elements shown in the FIGs., including functional blocks labeled as "processors", may be provided through the use of dedicated hardware as well as hardware capable of executing software in association with appropriate software. When provided by a processor, the functions may be provided by a single dedicated processor, by a single shared processor, or by a plurality of individual processors, some of which may be shared. Moreover, explicit use of the term "processor" or "controller" should not be construed to refer exclusively to hardware capable of executing software, and may implicitly include, without limitation, digital signal processor (DSP) hardware, read-only memory (ROM) for storing software, random access memory (RAM), and non-volatile storage. Other hardware, conventional and/or custom, may also be included. Similarly, any switches shown in the FIGS. are conceptual only. Their function may be carried out through the operation of program logic, through dedicated logic, through the interaction of program control and dedicated logic, or even manually, the particular technique being selectable by the implementer as more specifically understood from the context.

[0010] In the claims hereof any element expressed as a means for performing a specified function is intended to encompass any way of performing that function including, for example, a) a combination of circuit elements which performs that function or b) software in any form, including, therefore, firmware, microcode or the like, combined with appropriate circuitry for executing that software to perform the function. The invention as defined by such claims resides in the fact that the functionalities provided by the various recited means are combined and brought together in the manner which the claims call for. Applicant thus regards any means which can provide those functionalities as equivalent as those shown herein.

[0011] Unless otherwise explicitly specified herein, the drawings are not drawn to scale.

[0012] FIG. 1 shows, in flowchart form, an exemplary process for developing an orthogonal training sequence can be developed for a channel that is described as a finite impulse response (FIR) filter having a length M_{new} from already existing orthogonal training sequences for at least two channels that have respective lengths M_{old1} and M_{old2} each that is less than M_{new} such that the product of M_{old1} and M_{old2} is equal to M_{new} when M_{old1} and M_{old2} have no common prime number factor. The process is entered in step 101 when a new training sequence is required, e.g., when developing a new wireless communication system. Next, in step 103, two already existing orthogonal training sequences old1 and old2 for at least two channels that have respective lengths M_{old1} and M_{old2} each that is less than M_{new} such that the product of M_{old1} and M_{old2} is equal to M_{new} when M_{old1} and M_{old2} have no common prime number factor is selected. If it is not possible to find values such that the product of M_{old1} and M_{old2} is equal to M_{new}, e.g., M_{new} is a prime number, then the process must terminate in an error condition. However, from a practical point of view, typically using a larger value of M_{new} rather than the exact value of M_{new} being sought will yield adequate results.

[0013] The initial orthogonal sequences may be obtained by performing an exhaustive search over each possible combination for a particular modulation scheme's alphabet and a given channel length to determine the existence of an orthogonal training sequence. Not all such searches will yield an orthogonal sequence, e.g., no such sequence has yet been found for a channel length of 13. Also, the time required to conduct each such searches may be quite long. Those orthogonal sequences that have been found to date are shown in Table 1. In particular, Table 1 shows exemplary orthogonal sequences and the corresponding lengths and modulation schemes for which they were found. Note that Table 1 also includes the length 4 and length 16 orthogonal sequences that were known in the prior art.

TABLE 1

Length	Modulation Scheme	Orthogonal Sequence
M=2	QPSK	1,-j
M=3	PAM	-2,-2,1
M=3	V.29	-3, 3+3j,3+3j

TABLE 1 (continued)

Length	Modulation Scheme	Orthogonal Sequence
M=4	BPSK	1,1,1,-1
M=5	No name	2,2,2,2,-3
M=5	V.29	-3+3j,-3j,-3+3j,3+3j,3+3j
M=6	PAM	-1,1,-1,1,-1,-2
M=6	16QAM	-3+3j,-1+3j,-1-j,1-3j,-1+3j,-1-j
M=6	V.29	3-3j,-3,3-3j,3+3j,3j,3+3j
M=7	PAM	-2,-2,-1,1,1,-2,1
M=7	V.29	1-j,1-j,1-j,1-j,1-j,1-j,5j
M=8	QPSK	1,-j,1,-1,-1,-j,-1,-1
M=9	No name	2,2,2,2,2,2,2,2,-7
M=9	PAM	-2,-8,1,-2,1,1,-2,1,1
M=9	V.29	-3-3j,-3+3j,3,-3+3j,-3-3j,3+3j,3+3j,3+3j,3+3j
M=10	16QAM	3-j,3+j,3-j,-3+3j,1+3j,-1-j,-3+j,-1-j,1+3j,-3+3j
M=12	PAM	-2,-2,-2,-1,1,-2,-2,2,-2,1,1,2
M=12	16QAM	-3-j,-1-j,1-j,-1-j,1+3j,3-3j,-3-j,-1-j,-3+3j,-1-j,1+3j,-3+3j
M=15	PAM	2,-2,-2,1,-2,2,1,1,-2,1,2,1,1,1,1
M=16	QPSK	1,1,1,1,1,j,-1,-j,1,-1,1,-1,1,-j,-1,j
M=18	PAM	2,-2,1,-2,1,1,-1,1,1,-2,-2,1,2,1,1,1,1,1
M=18	V.29	-3-3j,-3+3j,3,-3+3j,-3-3j,3+3j,3+3j,3+3j,3+3j,3-3j, -3-3j,3j,-3-3j,3-3j,-3+3j,-3+3j,-3+3j,-3+3j
M=19	PAM	-2,-2,1,2,-2,1,1,-2,-2,-2,-2,1,-2,1,-2,1,1,1,1
M=21	PAM	-2,1,-2,1,1,1,1,-2,-2,1,1,-2,1,1,1,1,1,1,1,1,1,1,1

[0014] Thereafter, in step 105, the training sequence old1 is repeated M_{old2} number of times to form a first concatenated sequence. Similarly, the training sequence old2 is repeated M_{old1} number of times to form a second concatenated sequence, so that both the first concatenated sequence and the second concatenated sequence have the same length which is the desired sequence length M_{new}. For example, if M_{old1} is 3 using PAM and M_{old2} is 7 using PAM a sequence with length M_{new} equal to 21 can be formed. Table 2 shows the concatenated sequence formed for M_{old1} being 3 using PAM and M_{old2} is 7. Table 3 shows M_{old2} is 7 using PAM and M_{old1} being 3.

Table 2

-2	-2	1	-2	-2	1	-2	-2	1	-2	-2	1	-2	-2	1	-2	-2	1	-2	-2	1

Table 3

-2	-2	-1	1	1	-2	1	-2	-2	-1	1	1	-2	1	-2	-2	-1	1	1	-2	1

[0015] In step 107, each term of the first concatenated sequence is multiplied by the correspondingly located term in the second concatenated sequence and the resulting product is placed in the same corresponding location in a new sequence made up of the resulting M_{new} products. This new sequence is an orthogonal sequence of length M_{new}. Table 4 shows the resulting new training sequence that is formed from the products of the terms of Tables 2 and 3, where M_{new} is 21. Note that this new training sequence for $M_{new} = 21$ is different than the training sequence found by computer search for M=21.

Table 4

4	4	-1	-2	-2	-2	-2	4	-2	2	-2	1	4	-2	-2	4	2	1	-2	4	1

[0016] The process then exits in step 109.

[0017] If there is more than one existing orthogonal sequence for a particular length channel, e.g., there may be different orthogonal sequences for different modulation schemes for the same length channel, the implementer may choose which ever orthogonal sequence gives the results desired. Often, for practical applications, the result that yields the modulation scheme that is most suitable for use with the actual channel, which may yield the highest speeds, or the result that yields the smallest alphabet, which would reduce the hardware required for implementation, is desirable.

[0018] Table 5 shows several additional exemplary training sequences that were obtained using the procedures of the instant invention.

Table 5

M=14	V.29	1-j,-1-j,1-j,-1-j,1-j,-1-j,5j,-1-j,1-j,-1-j,1-j,-1-j,1-j,-5
M=20		2,2,2,-2,-3,2,2,-2,2,-3,2,-2,2,2,-3,-2,2,2,2,3

[0019] FIG. 2 shows exemplary receiver 200 in accordance with the principles of the invention. Receiver 200 computes

$$\mathbf{w}_{k+1} = \mathbf{w}_{k-1} + \mu \sum_{p=0}^{I} \mathbf{x}^{*}_{k-p} \, e(k-p|k-p),$$

where X contains the M elements of the training sequence starting at time instant k-p, where k is the absolute time and p is the relative lag thereto, * means conjugate complex, and e() is the error using X_{k-p} and W is the channel estimate. Shown in FIG. 2 are a) parallel weight computers 201, including parallel weight computers 201-1 through 201-M; b) adder 203, c) multiplier 205 and d) new weight vector producer 207.

[0020] In order to enjoy a computation efficiency over the prior art, there are at least 2 parallel weight computers 201, and there are no more than M parallel weight computers 201, where M is the channel length. Each of parallel weight computers 201 computes $x_{k-p} e(k-p|k-p)$. To this end, each of parallel weight computers 201 receives the training sequence X and d(k) which is the actual received symbol at time k, as well as the latest value of the weight vector W. Note that, more particularly, $e(k|k) = d(k) - x_k^T w_k$ where T means transpose. Also note that X and W are vectors while d(k) is a scalar.

[0021] Adder 203 sums the outputs of each of parallel weight computers 201, i.e., each corresponding position of the vectors that are output by parallel weight computers 201 are summed. The summation vector produced as an output by adder 203 is supplied to multiplier 205 which multiplies each element of the summation vector by the step size μ, thus scaling the summation vector by μ. The scaled summation vector is then supplied to new weight vector producer 207, which adds the scaled summation vector to the previously produced weight vector, which was stored in new weight vector producer 207, and supplies the resulting value as the new weight, as well as storing it.

[0022] Note that the orthogonal sequences referred to herein as orthogonal training sequences need not actually ever have been used for training, although typically they are suitable for use as training sequences. Furthermore, the orthogonal sequences may be used for synchronization purposes.

Claims

1. A method for developing a new orthogonal sequence for a channel of length M_{new}, the method comprising the steps of:

   selecting first and second existing orthogonal sequences old1 and old2 for at least two channels that have respective lengths M_{old1} and M_{old2}, the product of M_{old1} and M_{old2} being equal to M_{new} and M_{old1} and M_{old2} having no common prime number factor;

   repeating the sequence old1 M_{old2} number of times to form a first concatenated sequence;

repeating the sequence old2 M_{old1} number of times to form a second concatenated sequence;
multiplying each term in said first concatenated sequence by a correspondingly located term in said second concatenated sequence; and
forming said new sequence by placing each product produced in said multiplying step into a corresponding location therein.

2. The invention as defined in claim 1 further comprising the step of performing a search over each possible combination for a particular modulation scheme's alphabet and a given channel length to determine the existence of an orthogonal sequence for use in said selecting step.

3. The invention as defined in claim 1 wherein at least one of said first existing orthogonal sequence, said second existing orthogonal sequence, and said new orthogonal sequence is employed as a training sequence.

4. The invention as defined in claim 1 wherein at least one of said first existing orthogonal sequence, said second existing orthogonal sequence, and said new orthogonal sequence is employed as a synchronization sequence.

5. The invention as defined in claim 1 wherein first and second existing orthogonal sequences each have a length that has no common prime number factor with the other.

6. An new orthogonal sequence which is developed as a function of first and second existing orthogonal training sequences.

7. The invention as defined in claim 6 wherein said new orthogonal sequence is for a channel of length M_{new}, and said function for developing said new orthogonal sequence comprises the steps of:

selecting said first and second existing orthogonal sequences old1 and old2 for at least two channels that have respective lengths M_{old1} and M_{old2}, the product of M_{old1} and M_{old2} being equal to M_{new} and M_{old1} and M_{old2} having no common prime number factor;
repeating the sequence old1 M_{old2} number of times to form a first concatenated sequence;
repeating the sequence old2 M_{old1} number of times to form a second concatenated sequence;
multiplying each term in said first concatenated sequence by a correspondingly located term in said second concatenated sequence; and
forming said new orthogonal sequence by placing each product produced in said multiplying step into a corresponding location therein.

8. The invention as defined in claim 6 wherein first and second existing orthogonal sequences each have a length that has no common prime number factor with the other.

9. A receiver adapted for use with a new orthogonal sequence that was developed as a function of first and second existing orthogonal sequences.

10. The invention as defined in claim 9 wherein said new orthogonal sequence is a training sequence and said receiver is adapted to use an optimal step size that results in fastest possible training.

11. The invention as defined in claim 9 wherein said new orthogonal sequence is a training sequence and said receiver is adapted to use a step size $\mu_o = 1 / \| X_k \|$ for training, where X_k is a vector containing M elements of the training sequence and $\| X_k \|$ denotes the squared norm of X_k.

12. The invention as defined in claim 9 wherein said new orthogonal sequence is for a channel of length M_{new}, and said function for developing said new orthogonal sequence comprises the steps of:

selecting said first and second existing orthogonal sequences old1 and old2 for at least two channels that have respective lengths M_{old1} and M_{old2}, the product of M_{old1} and M_{old2} being equal to M_{new} and M_{old1} and M_{old2} having no common prime number factor;
repeating the sequence old1 M_{old2} number of times to form a first concatenated sequence;
repeating the sequence old2 M_{old1} number of times to form a second concatenated sequence;
multiplying each term in said first concatenated sequence by a correspondingly located term in said second concatenated sequence; and forming said new orthogonal sequence by placing each product produced in

said multiplying step into a corresponding location therein.

13. The invention as defined in claim 9 wherein first and second existing orthogonal sequences each have a length that has no common prime number factor with the other.

14. The invention as defined in claim 9 wherein said receiver computes

$$\mathbf{w}_{k+1} = \mathbf{w}_{k-1} + \mu \sum_{p=0}^{I} \mathbf{x}^{*}_{k-p}\, e(k-p|k-p)$$

where X contains M elements of said new orthogonal sequence starting at time instant k-p, where k is the absolute time and p is the relative lag thereto, * means conjugate complex, and e() is the error using X_{k-p}, W is the weight vector that represents the channel estimate, and μ is the step size.

15. The invention as defined in claim 9 wherein said receiver comprises:

a plurality of parallel weight computers;
an adder coupled to receive and add the outputs of said parallel weight computers;
a multiplier for scaling by a step size a vector produced as an output by said adder; and
a new weight vector producer for supplying as an output a new weight vector as a function of a previously produced weight vector and a scaled vector supplied by said multiplier.

FIG. 1

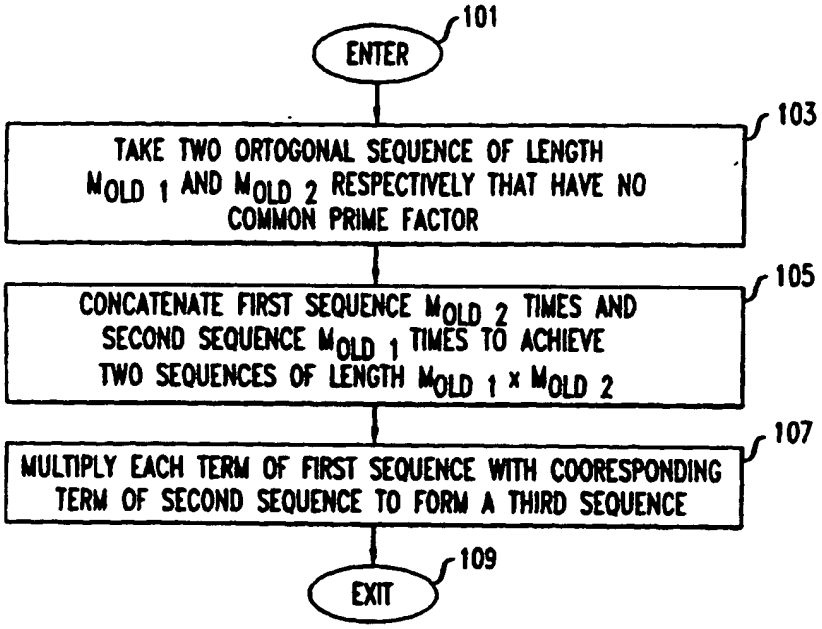
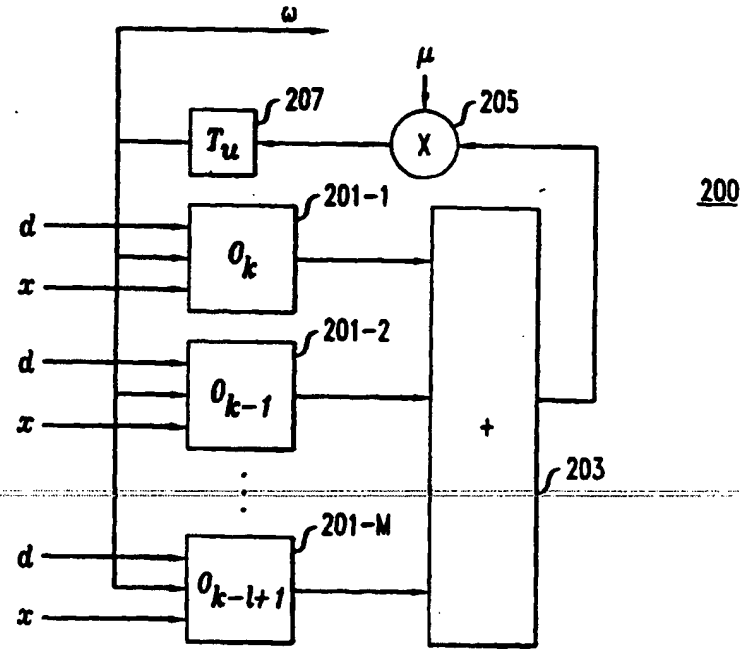

101
ENTER
103
TAKE TWO ORTOGONAL SEQUENCE OF LENGTH $M_{OLD\ 1}$ AND $M_{OLD\ 2}$ RESPECTIVELY THAT HAVE NO COMMON PRIME FACTOR
105
CONCATENATE FIRST SEQUENCE $M_{OLD\ 2}$ TIMES AND SECOND SEQUENCE $M_{OLD\ 1}$ TIMES TO ACHIEVE TWO SEQUENCES OF LENGTH $M_{OLD\ 1} \times M_{OLD\ 2}$
107
MULTIPLY EACH TERM OF FIRST SEQUENCE WITH COORESPONDING TERM OF SECOND SEQUENCE TO FORM A THIRD SEQUENCE
109
EXIT

FIG. 2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EUROPEAN SEARCH REPORT

Application Number
EP 01 30 2240

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	DINAN, JABBARI: "Spreading codes for direct sequence DMA and wideband CDMA cellular networks" IEEE COMMUNICATIONS MAGAZINE, vol. 36, no. 9, September 1998 (1998-09), pages 48-54, XP000784826 Piscataway, US ISSN: 0163-6804 * section "Kasami Sequences" *	1-14	H04L25/03 H04J13/00
X	"Proposal for RACH preambles" REPORT OF TSG-RAN WORKING GROUP 1 MEETING #6, 'Online! 7 August 1999 (1999-08-07), XP002174961 Retrieved from the Internet: <URL:http://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_06/Docs/Pdfs/r1-99893.pdf> 'retrieved on 2001-08-13! * sectoin 2.0 *	1-14	
A	KUGANESAN ET AL.: "Multicode modulation for high-speed wireless data transmission" IEEE INTERNATIONAL SYMPOSIUM ON PERSONAL, INDOOR AND MOBILE RADIO COMMUNICATIONS, 1 - 4 September 1997, pages 457-461, XP002174939 New York, US ISBN: 0-7803-3871-5 * page 458, left-hand column, paragraph 1 * * page 459, left-hand column, paragraph 4 * * page 459, right-hand column, paragraph 3 *	1-14	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H04L H04J

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15 August 2001	Scriven, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

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Application Number
EP 01 30 2240

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	DONELAN, O'FARRELL: "Method for generating sets of orthogonal sequences" ELECTRONICS LETTERS, vol. 35, no. 18, 2 September 1999 (1999-09-02), pages 1537-1538, XP006012622 Stevenage, GB ISSN: 0013-5194 * page 1537, left-hand column, paragraph 2 *	1-14	
A	LIAU, WEI: "Orthogonal LMS algorithms for fast line echo canceller training" IEEE SOUTHEASTCON , 11 - 14 April 1996, pages 444-446, XP002174940 New York, us ISBN: 0-7803-3088-9 * page 1, right-hand column, paragraph 2 *	1	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)

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L : document cited for other reasons

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